REMARKS

Applicant respectfully requests reconsideration of the present application in view of this Amendment.

It is believed that this Amendment does not raise new issues that would require further consideration and/or search, and also does not raise the issue of new matter. It is also believed and respectfully submitted that this Amendment places the application in better form for appeal by materially reducing or simplifying the issues for appeal.

On page two (2) of the Final Office Action, claims 13, 14, 16 to 19, 21 and 25 were rejected under 35 U.S.C. §102(b) as anticipated by Rosnowski, U.S. Patent No. 4,099,997 (Rosnowski).

Applicants respectfully disagree with the analysis of the Rosnowski reference presented in the Final Office Action, and maintain that independent claim 13, and dependent claims 14, 16 to 19, 21 and 25, are not anticipated by Rosnowski.

In particular, it is respectfully submitted that the statement in the Final Office Action that Rosnowski discloses heating the semiconductor wafer to a high temperature (at col. 2, lines 44-45) while the glass layer is applied so that the dopant from the solid glass layer penetrates into the semiconductor wafer to produce the at least one doped region is incorrect.

The Rosnowski reference purports to concern depositing a silicon dioxide layer over a wafer having borosilicate glass layers on either side and then annealing these layers at 900 degrees Celsius. (See Rosnowski, col. 2, lines 34-48). The annealing assertedly produces a "surface" concentration of boron impurities on the wafer (see col. 3, lines 14 to 18), and after this initial annealing, the borosilicate glass is then removed. (See col. 3, line 40).

There is a clear difference between heating at 900 degrees in the presence of doped glass to produce a surface concentration and heating at a high temperature, i.e., at least 1200 degrees, to have the dopant penetrate the layer. The withdrawal of the prior § 112 rejection with respect to the term "high temperature" in view of the previous response to the first Office Action indicates the Office's acknowledgment that "high temperature" as recited in claim 13 refers to a temperature greater than 1200 degrees Celsius in light of the clear guidance within the specification. The heating at this higher temperature results in the dopant being driven deeper into the semiconductor. The fact that the higher temperature of 1200 degrees is required to drive dopants deeper into the semiconductor wafer is confirmed by the Rosnowski reference itself, which states that after the borosilicate glass is removed, the

"wafer is then heated to a temperature at which the first impurities and the second impurities are driven further thereinto." (Col. 3, lines 42 to 44). This secondary heating temperature turns out to be similar to the "high temperature" claimed of 1200 to 1300 degrees Celsius. Thus, since the reference in Rosnowski to an initial annealing at 900 degrees (at which point the semiconductor wafer is in contact with the borosilicate glass layer) does not drive the dopants into the semiconductor wafer but merely produces a surface concentration, it cannot be said that Rosnowski identically describes (or even suggests) heating the semiconductor wafer to a high temperature while the glass layer is applied so that the dopant from the solid glass layer penetrates into the semiconductor wafer to produce the at least one doped region prior to removal of the glass layer.

For at least these reasons, it is respectfully submitted that Rosnowski does not anticipate claim 13, or claims 14, 16 to 19, 21 and 25, which depend from claim 13.

On page three (3) of the Office Action, claims 15, 22 and 28 were rejected under 35 U.S.C. § 103(a) as unpatentable over Rosnowski in view of Schwalke, U.S. Patent No. 5,496,765 (Schwalke).

To reject a claim as obvious under 35 U.S.C. § 103, the prior art must disclose or suggest each claim element and it must also suggest combining the elements in the manner contemplated by the claim. (See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296 (1990)).

Each of claims 15, 22 and 28 depend from and incorporate the features of independent claim 13. The secondary Schwalke reference purportedly relates to a method for producing an insulating trench in an SOI substrate, and refers to diffusion of dopants laterally through side walls of an etch. As characterized in the reference, the dopant diffuses from a glass layer through intermediary silicon dioxide films to a monocrystalline layer and does not diffuse to the substrate layer. (See Schwalke, col. 4, lines 38 to 47). Since Schwalke also does not disclose or suggest heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates *into the semiconductor wafer* (i.e., the substrate) as recited in claim 13, it is respectfully submitted that it does not cure the critical deficiencies of the primary Rosnowski reference discussed above, and therefore the references relied upon do not disclose or suggest each of the features of claims 15, 22 and 28 as required. For at least this reason, it is respectfully submitted that the obviousness rejections of claims 15, 22 and 28 should be withdrawn.

On page four (4) of the Office Action, claims 20, 23, 24, 29 and 30 were rejected

under 35 U.S.C. § 103(a) as unpatentable over Rosnowski and further in view of Evans Jr. et al., U.S. Patent No. 4,104,091 (Evans, Jr.) and Weijland, U.S. Patent No. 3,907,615 (Weijland).

The Final Office Action admits that Rosnowski does not disclose or suggest doping opposite sides of a semiconductor wafer with opposite types of doping, but then asserts that when Rosnowski is viewed in combination with Evans, Jr. and Weijland that one of skilled in the art would arrive at the subject matter of claims 20, 23, 24, 29 and 30. It is respectfully submitted that the skilled practitioner would not be motivated to combine the references in the manner suggested in the Final Office Action.

The Final Office Action admits that neither Rosnowski and Evans, Jr. disclose or suggest heating a doped glass layer applied to a semiconductor wafer to a high temperature so that the dopant penetrates deeply into the semiconductor. As explained above, Rosnowski does not perform this step, and the diffusion process described in Evans takes place at a lower temperature of 900 degrees Celsius. (See Evans, col. 6, lines 13 to 20).

While Weijland purports to concern heating a doped glass layer applied to a semiconductor substrate, it actually refers to the fact that in portions of a substrate covered by a doped glass layer having a relatively high concentration of dopant, the dopant will be driven deeper upon heating at a particular temperature than in exposed portions, to which a doped silicon powder having a lower concentration is applied. There is no suggestion that heating the doped glass layer at a given concentration, in general, drives the dopant deeply into the substrate. In other words, the skilled practitioner would not be able to discern the effects of the heating at the prescribed temperature and duration from the effects of the differences in concentration. This lack of a proper suggestion is crucial, since the primary Rosnowski and secondary Evans references clearly do not provide any hint concerning heating a doped glass layer at a high temperature to have the dopant penetrate the substrate. Thus, Weijland may only indicate to the skilled practitioner to "try" to arrive at the subject matter of claims 20, 23, 24, 29 and 30. However, the cases of In re Fine, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988), and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain an "obvious to try" standard does not reflect the proper evidence to support an obviousness rejection.

For at least these reasons, it is respectfully submitted that claims 20, 23, 24, 29 and 30 are allowable over the references relied upon.

On page five (5) of the Office Action, claims 26 and 27 were rejected under 35 U.S.C. § 103(a) as unpatentable over Rosnowski in view of Shinohara, JP 59-80928.

The Shinohara reference purportedly refers to forming a non-doped glass layer over a doped substrate. It is respectfully submitted, however, that any review of the Shinohara reference makes plain that it simply does not disclose or suggest heating the semiconductor wafer to a high temperature so that the dopant from the solid glass layer penetrates into the semiconductor wafer as recited in claim 13. Accordingly, it does not cure the critical deficiencies of the primary Rosnowski reference. It is therefore respectfully submitted that claims 26 and 27 are allowable over the references relied upon.

CONCLUSION

In view of all the above, it is believed that rejections of claims 13 to 30 have been obviated, and that currently pending claims 13 to 30 are allowable. It is therefore respectfully requested that the rejections be reconsidered and withdrawn, and that the present application issue as early as possible.

Respectfully submitted,

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Dated: 3/5/03

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AMENDMENT VERSION WITH MARKINGS

IN THE CLAIMS:

Please add new claims 29 and 30 as indicated above, and please amend without prejudice claim 13 as follows:

13. (Amended) A method for producing a semiconductor component in which at least one doped region is introduced into a semiconductor wafer, comprising the steps of:

applying a solid glass layer provided with a dopant on at least one of two sides of the semiconductor wafer;

heating the semiconductor wafer to a high temperature while the glass layer is applied so that the dopant from the solid glass layer penetrates into the semiconductor wafer to produce the at least one doped region;

removing the solid glass layer; and

providing the dopant at a dosage of at least $10^{17}/cm^2$ in the at least one doped region.